IN THE SPECIFICATION

Please replace the paragraph at page 2, lines 3-15 with the following rewritten paragraph:

When being configured by a CMOS circuit, a conventional voltage level shifter has the following configuration. Two pairs of serial circuits of P-channel MOSFETs (hereinafter, referred to as "PMOSs") and N-channel MOSFETs (hereinafter, referred to as "NMOSs"), which are connected to high voltage power supply, are provided. Drain output ends of the PMOSs are mutually connected to ~~gates~~ gate electrodes (hereinafter, referred to as "gates") of the PMOSs of the other pair. Signals with low voltage level amplitude and mutually reversed polarities are inputted into gates of the NMOSs. Output signals with high voltage level are obtained from the drain output end of one of the PMOSs (e.g., refer to Yasoji Suzuki, "Applied Technique of CMOS", Fifth Edition, Sanpo Publications Inc., February 15th, 1982, p29 - 30).

Please replace the paragraph at page 3, lines 1-6 with the following rewritten paragraph:

Level changer 101 has a PMOS 113, a PMOS 114, an NMOS 123, and an NMOS 124. ~~Sources~~ Source electrodes (hereinafter, referred to as "sources") of PMOS 113 and PMOS 114 are connected to a high voltage power supply VDD2. A source of NMOS 123 and NMOS 124 is connected to a reference potential VSS. ~~Drains~~ Drain electrodes (hereinafter, referred to as "drains") of PMOS 113 and NMOS 123 are connected to each other. Drains of PMOS 114 and NMOS 124 are connected to each other.